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Abstract— **A new fabrication process is described for high-performance embedded or integrated inductors for power converters. The process includes etching V-grooves in a silicon substrate, depositing granular composite magnetic materials, and electroplating copper conductors.**

I. Introduction

Inductors are essential components for efficient power conversion, but high-performance inductors are not available in conventional integrated circuit or packaging technologies. We have proposed designs for high-performance thin-film power inductors fabricated on a silicon substrate [1], [2]. These inductors could be embedded in thin-film packaging or integrated on the same die as silicon power devices, leading to a complete power converter in a single package in either case. In this paper we detail the proposed fabrication process and report progress on improved magnetic material deposition.

Although many prototype microfabricated thin-film magnetic components have been reported [3-19], most are limited by low efficiency (often 60% or lower) and low power density (often under 1 W/cm^2 of substrate area). This is not adequate for the emerging challenges in microprocessor power delivery: high current requirements (up to 100 A or more) supplied efficiently at voltages near 1 V, with the requirement that the voltage must remain stable despite rapid changes in load current. The inductor is associated with fundamental performance constraints in a buck-converter for this application, and thus it is crucial to high-performance power delivery [1]. We have proposed microfabricated designs that can meet these requirements using new granular composite magnetic materials that reduce losses and a V-groove geometry to improve efficiency and power density [1], [2]. The designs are specifically optimized for performance in microprocessor power delivery, resulting in a predicted power density of 158 W/cm^2 and 95% efficiency for an 8 MHz, 3.6 V to 1.1 V converter. In the following sections we describe the deposition of the magnetic materials and the complete inductor fabrication process.

II. Magnetic Materials

Microfabricated magnetic components are often made with thin layers of magnetic material to reduce eddy current losses. This is effective at controlling loss resulting from flux travelling in the plane of the film, but flux components out of the plane can still induce eddy currents that result in substantial losses [2], [20]. An alternative is to use fine particles of metallic magnetic material instead of multilayer thin films, similar in concept to conventional powdered iron materials. Although conventional powdered-metal materials have limited power performance at frequencies in the range above 1 MHz, recent work has shown that higher performance is possible in vacuum deposited materials with nanoscale particles of Co or Fe [21], [22], [23], [24], [25]. These materials have traditionally been fabricated by reactive sputtering. A target such as Co-Al is sputtered in an atmosphere containing a reactive gas such as O_2. Ideally, the aluminum combines with the oxygen and the cobalt forms a separate phase. The resulting material can have high performance at high frequencies, including relative permeability of 170 and Q of 60 at 100 MHz, with permeability maintained to about 1 GHz [24], attractive properties for both power and RF applications. In [18], an inductor application of these materials in an efficient high-frequency dc-dc converter was demonstrated at low power density. Such materials could be applied in improved designs to achieve much higher power density [1], [2].

We are currently studying several alternative methods of depositing such materials. We have demonstrated that thermal evaporation can be used to produce similar materials using Co and MgF_2 [25]. However, the process was not well controlled and has demonstrated poor repeatability. A new vacuum system for this process with a lower base pressure and an e-beam source for Co evaporation is being tested. A sputtering system using a composite Al_2O_3/Co target is also being tested. This system has also produced good soft magnetic films. Coercivity, a critical parameter for low-loss inductors, is seen to decrease with vacuum base pressures below 10^{-6} Torr.

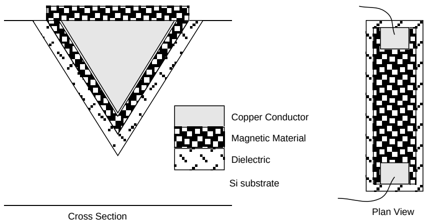

Fig. 1. Schematic diagram of V-groove inductor. Contact pads are indicated on the plan view by "bond wires", but in practice the interconnection would be accomplished with another metal layer or solder bumps, to avoid high impedance and stray inductance associated with bond wires.

III. Fabrication

In this section the fabrication process for the inductor is described. The proposed inductor design is in the form of a triangular wire surrounded by magnetic material, embedded in a silicon substrate, as sketched in Fig. 1. The process is based on a V-trench formed by anisotropic etching of the silicon substrate. Composite magnetic material is deposited in the trench to form the core. Copper is filled in the groove to form the conductor and an overlayer of core material completes the inductor. The magnetic material is wrapped around a single wire and forms a one-turn inductor. Detailed design calculations for such inductors for microprocessor power delivery applications are discussed in [1], [2]; inductors about 500 μm wide and 350 μm deep should be sufficient for such applications. Our initial fabrication tests are limited to smaller inductors 270 μm wide and 190 μm deep, in order to allow fabrication on standard-thickness three-inch silicon wafers.

The first step in the proposed fabrication process is to grow a masking layer to be used for the anisotropic etch of the V-groove. Thermally grown SiO_2 is good for this purpose because it forms without defects. We used a combination of wet and dry oxidation to grow 1.5 μm of oxide. This oxide layer is then patterned using HF to form the mask for the anisotropic etch.

Anisotropic etchants of silicon include potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), and ethylene diamine pyrocatechol (EDP). KOH is used as etchant for our process [26], [27]. The

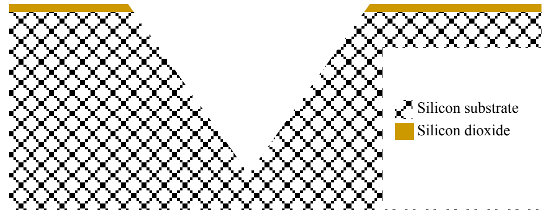

Fig. 2. Cross section showing the etched V-groove in a silicon substrate.

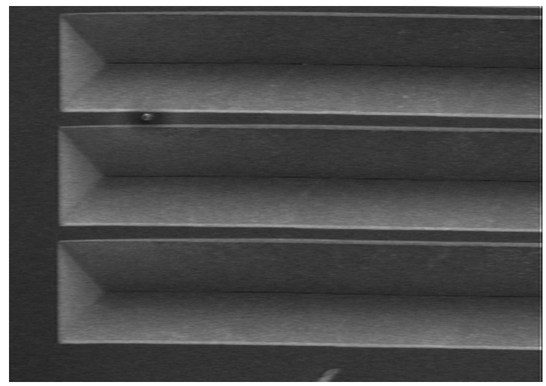

Fig. 3. SEM image showing the etched V-grooves in a silicon substrate.

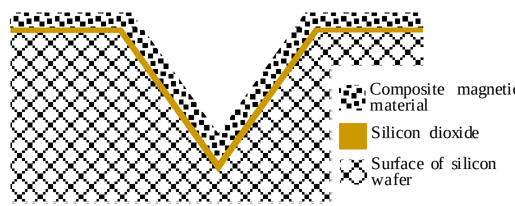

Fig. 4. Cross section showing the etched V-groove with two layers deposited on top of it: an insulating oxide layer followed by composite magnetic material.

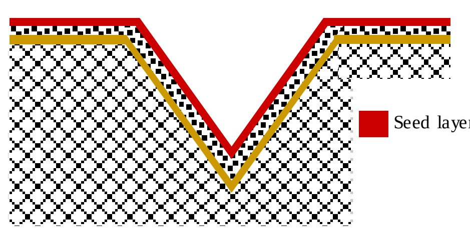

Fig. 5. A thin conductive metal seed layer that will be used for electroplating is deposited over the full wafer surface.

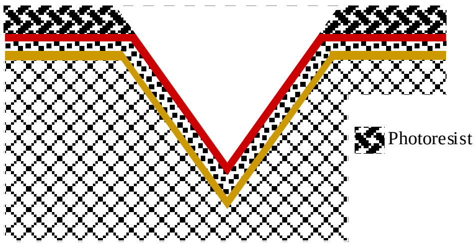

Fig. 6. Photoresist is spun and developed to expose the seed layer in the V-grooves.

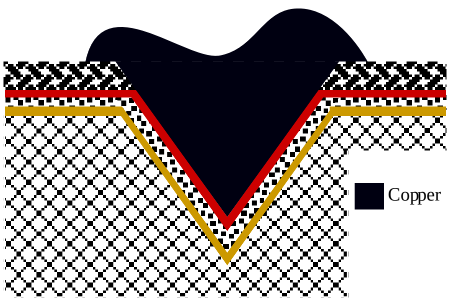

Fig. 7. Copper is electroplated into the V-grooves with the help of the seed layer.

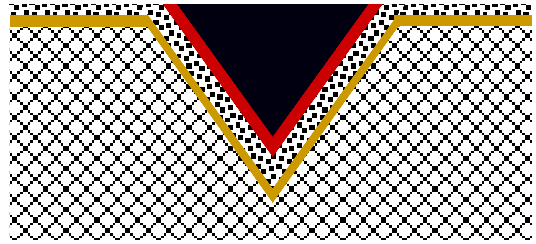

Fig. 8. A planarized wafer surface is achieved by chemical mechanical polishing to remove excess copper from electroplating.

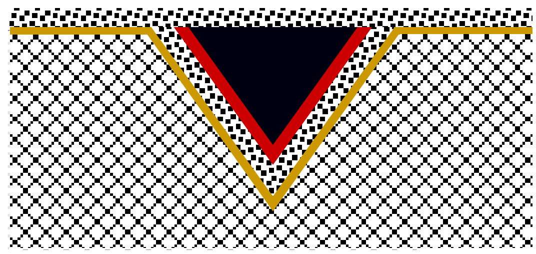

Fig. 9. More magnetic material is deposited to complete the V-groove inductor.

etch rates of various planes of silicon in an anisotropic etchant are found to decrease in the order $\{100\} > \{110\} > \{111\}$. The slowest etching planes are exposed as etching progresses [26]. We use (100) wafers. If the mask opening is accurately aligned with the primary orientation flat, i.e., the [110] direction, after prolonged etching the $\{111\}$ family of planes is exposed down to their common intersection and the (110) plane disappears creating a V-groove with $<111>$ oriented sidewalls at 54.74° to the (100) surface as shown in Fig. 2 [26]. Fig. 3 shows a scanning electron microscope (SEM) image of the etched V-grooves.

An overhang of oxide around the periphery of the V-grooves is observed at the end of the anisotropic etch step. This could pose problems for the other steps of the fabrication process. The overhang is removed by etching all the remaining oxide on the wafer with HF. The next step is to grow another layer of silicon dioxide. The oxide layer will help in electrically isolating inductors from other devices on the same substrate. Composite magnetic material can be deposited on this oxide layer by one of the methods discussed in Section II. The thickness of the core will be about 10 μm. The result of the first steps discussed above is shown in Fig. 4.

Copper deposition is the next step in the fabrication. A thin seed layer of metal is deposited over the entire wafer surface (Fig. 5). Photoresist is then spun on top of the wafer and developed to expose the V-grooves as shown in Fig. 6. Copper can be electroplated into the grooves with the help of the seed layer. The electroplating is stopped when the copper grows out and overfills the groove as shown in Fig. 7. The excess copper can be removed by chemical mechanical polishing. The polishing is continued until the seed layer outside the groove is removed and the core is exposed (Fig. 8). More magnetic material can then be deposited as the next step to complete the core around the copper as shown in Fig. 9. Contacts have to be placed through the core to make connections with the underlying copper. Laser ablation can be used to remove magnetic material where contacts are needed. This contact area can be used for various on-chip or inter-chip interconnect strategies. For example, solder bumps could be grown, and the inductor could then be connected to other chips using flip-chip technology.

IV. Conclusion

Inductor designs based on the V-trench process, using high-performance composite magnetic materials, are expected to enable compact low-profile microprocessor power converter circuits. Both vacuum evaporation and sputtering show promise as fabrication methods for the magnetic materials. A fabrication process for the inductors has been proposed. These improvements should allow much higher performance for embedded or integrated magnetic components in power applications.

V. Acknowledgments

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