Improved Distributed Model for Capacitors in High-Performance Packages

C. R. Sullivan
A. M. Kern

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Charles R. Sullivan, Yuqin Sun, and Alexandra M. Kern
charles.r.sullivan@dartmouth.edu yuqin.sun@dartmouth.edu alexandra.m.kern@alum.dartmouth.org
http://engineering.dartmouth.edu/inductor
8000 Cummings Hall, Dartmouth College, Hanover, NH 03755, USA, Tel. +1-603-646-2851 Fax +1-603-646-3856

Abstract—***Time-domain and frequency-domain measurements show that a simple lumped RLC model for a multilayer ceramic capacitor is inadequate, overestimating high-frequency impedance by a factor of five. A lossy transmission-line model works better, and is improved by placing incremental resistance in series with the incremental capacitance. Refinements of this model are developed based on time-domain step-response measurements and on frequency-domain impedance measurements. Better packaging to reduce series inductance is discussed.***

I. Introduction

CONVENTIONALLY , capacitors are modelled as lumped RLC (resistor-inductor-capacitor) networks. The inductance includes inductance of the leads and inductance of the current path through the capacitor itself. When the lead inductance dominates, the lumped model is accurate. However, when the inductances of the paths through the capacitor itself dominate, an accurate model must be based on distributed capacitance and inductance [1], [2], [3]. Increasingly, where low inductance is important, packages with little or no lead inductance are used, and a distributed model becomes necessary if accuracy is needed. Capacitors with low-inductance packages include leadless multilayer ceramic (MLC) chip capacitors and similar stacked-film capacitors.

Frequently, the interconnect inductance for a capacitor is also significant, and when it dominates, a lumped RLC model for the combination of a capacitor and its interconnect path can be accurate. However, configurations with low interconnect inductance are increasingly common, such as in the careful board layouts needed for power delivery in high-current low-voltage digital systems, or low-inductance laminated bus-bar systems for high-power converters and inverters. Thus, the inductance of the capacitor itself is often important, and a true distributed model is needed.

The most basic distributed model is a simple lossless transmission line. This can lead to qualitatively and quantitatively useful information about capacitor behavior, and it can lead to simple and useful relationships between capacitor geometry and in-circuit performance [3]. However, the assumption of ideal transmission line behavior does not truly match the lossy behavior of typical practical capacitors. In this paper, several more detailed models are introduced and compared to experimental results for a 100 μF multilayer ceramic capacitor.

New experimental results also confirm that the equivalent series inductance (ESL) in a standard RLC capacitor model is misleading; with a distributed model, the only significant ESL is associated with packaging. In step-current measurements, the inductive effects are those that would be expected from the lead inductance alone, and can be greatly reduced with better packaging.

II. Lossless Transmission Line Model

Before considering a model for inductive effects in a capacitor, it is important to note that inductance cannot be defined except for a path forming a complete loop [4]. Thus, we must consider the impedance of a closed path including a capacitor. We consider a surface-mount capacitor on a thin two-layer board, with a current path across the top of the board, through the capacitor, down through vias to the bottom of the board, and returning under the capacitor. We define the impedance of the capacitor as the *difference* between the impedance of the complete loop just described and that of the same board with the capacitor replaced by a short[1].

A transmission line model for a capacitor in this configuration may be derived as in [3] by modelling the individual capacitor plate pairs as discrete capacitors, and then adding inductance between these capacitors. At a height x, the total inductance is

$$L = \mu_0 \frac{x\ell}{w} \tag{1}$$

where μ_0 is the permeability of free space, ℓ is the length of the capacitor (parallel to the current path), w is the width (parallel to the board but perpendicular to current flow), and we assume $w >> x$.

The result is a model in the form of a standard lumped transmission line model: a series of sections, each represented by the circuit in Fig. 1a. Ordinarily this model is considered a lumped approximation to a physically continuous transmission line. However, in this capacitor model, the individual elements in the lumped model represent the discrete capacitor plates. To remove the necessity to model the plates individually, this

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[1]This is equivalent to defining it as the impedance of the same configuration in the limit of zero board thickness and zero resistivity of the conductor on the board.

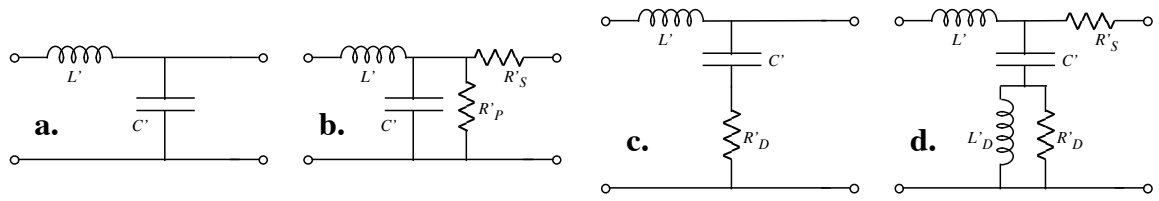

Fig. 1. Incremental sections of four transmission line models. a. Standard lossless. b. Standard lossy. c. A better representation of the origin of dissipation in a capacitor. d. The full model compared to experimental results. L'_D allows making the dissipation in R'_D frequency dependent.

lumped system is approximated by a continuous distributed transmission line model, as is done in both [1] and [3].

A useful way to describe a transmission line is in terms of characteristic impedance and the round-trip time for a wave traveling up the transmission line and back down. For a particular type of capacitor that has a given voltage rating, dielectric material, dielectric thickness, and plate thickness, we can describe the capacitance in terms of a constant capacitance per unit volume, C_v. The characteristic impedance then becomes [3]

$$Z_0 = \sqrt{\frac{L'}{C'}} = \sqrt{\frac{\mu_0 \ell / w}{C_v w \ell}} = \frac{1}{w}\sqrt{\frac{\mu_0}{C_v}}. \qquad (2)$$

The round trip time in terms of velocity v is $T = 2h/v$ and can be shown to be $T = 2h\ell\sqrt{\mu_0 C_v}$ [3].

When the assumption $w >> h$ does not hold, (2) cannot be expected to be accurate. In this case, either T or Z_0 can be measured experimentally, and the other calculated from the relationship $2Z_0C = T$. Alternatively, more extensive electromagnetic modelling could be used.

Other geometries, such as cylindrical capacitors with wound plates, require different models for good accuracy, although the qualitative results can be similar. For example, for cylindrical capacitors with coaxial terminations a rigorous distributed model was developed in the frequency domain in [1] and was further developed and applied in [5], [6].

III. Response to a Current Step and Improved Models

Consider a capacitor with a step change in current, as is often important in power electronics applications, as well as for a bypass capacitor in a digital system. The distributed model predicts a waveform like that shown in Fig 2. As the round trip time approaches zero, the steps merge into a ramp—the behavior of an ideal lumped capacitor.

In [3], several different capacitor responses were measured and compared to this model. The transmission line model was found to be much more accurate than the lumped RLC model. However, the actual steps are much less abrupt than those shown in Fig. 2. The use of a standard lossy transmission line model (a series connection of infinitesimal elements, each modelled as shown in Fig. 1b) was shown to help somewhat, but the smoothing effect was not fully satisfactory in matching the shape of the measured response.

The fact that Fig. 1b does not exactly match the measured behavior should not be surprising when the placement of resistances is compared with the physical system it is meant to represent. The parallel resistance R'_P represents leakage, which is

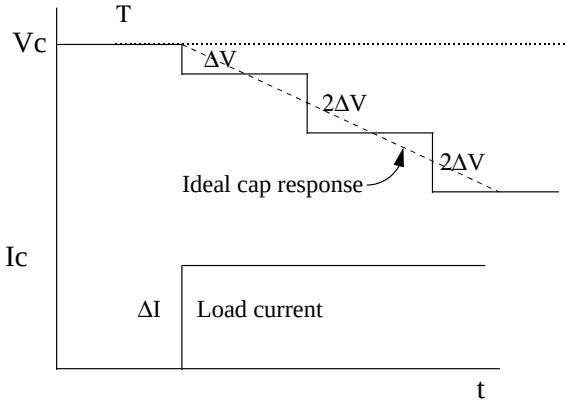

Fig. 2. Ideal distributed model behavior with current step.

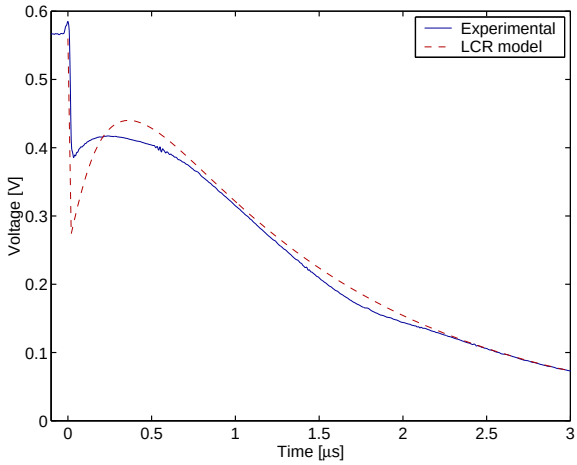

Fig. 3. Capacitor response to a step-like current waveform. The two curves are the measured voltage waveform on a 100 μF MLC capacitor and the simulated waveform using a lumped RLC model.

negligible in these capacitors. The series resistance R'_S would represent the resistance of the vertical path along the end metallization on the capacitor, which is very small. The model in Fig. 1c gives a much better match to measured results [2]. The resistor R'_D models both dielectric loss and the resistance of the metallization on each plate.

Fig. 1d shows a further improved model that was developed through comparison of measured and simulated step-response results. The inductor L'_D in parallel with R'_D was intended to achieve a frequency dependence in the loss effects, based on the idea that the losses in the ceramic dielectric increase rapidly with frequency. However, the values were chosen based on matching the overall step response of the system, not on measurements of dielectric characteristics, as will be discussed in Section V.

IV. Experimental Step-Response Measurements

Capacitors were tested by discharging them through a set of parallel MOSFETs, and monitoring their terminal voltages. The circuit was constructed on a double-sided copper-clad 50μm thick polyimide substrate for low inductance, with the main current path across the top, returning in parallel on the bottom. Four S08 packages containing eight IRF7103 MOSFETs were connected in parallel to minimize stray inductance in the MOSFETs. The inductance of the loop including the board, resistors, and MOSFETs, with the capacitor replaced by a copper foil short was measured as 1.4 nH. The capacitor was charged by an external voltage source through a relatively large resistor, and the MOSFETs were periodically pulsed on in order to allow observation of the capacitor voltage waveform during the transient. The data was saved with a digital oscilloscope, and later plotted along with simulation data.

A. Large multilayer ceramic capacitor

A 100 μF multilayer ceramic (MLC) capacitor was tested in this circuit with an estimated derivative of current greater than 1 A/ns, limited primarily by the inductance of the paralleled SO8 MOSFET packages.

Fig. 3 compares the measured voltage (at the solder connections of the capacitor to the board) to the simulated waveform using the lumped RLC model, with inductance based on the measured self-resonant frequency of 400 kHz. Here the spike predicted by the lumped model is much larger than in the measured data, showing that the contribution of ESL in the lumped model is misleading. The experiment also shows some non-uniformity in the voltage decay, tending toward stepped behavior, that is not captured at all by the lumped model.

In Fig. 4, the results of the improved lossy transmission line model are compared to the experimental results, showing a much better match. The left plot is again at the bottom of the capacitor, and the right plot is the voltage at the top of the capacitor, showing the expected shift in step timing between top and bottom. The initial spike is attributable to the fact that current initially crowds through the dielectric resistance (R'_D) of

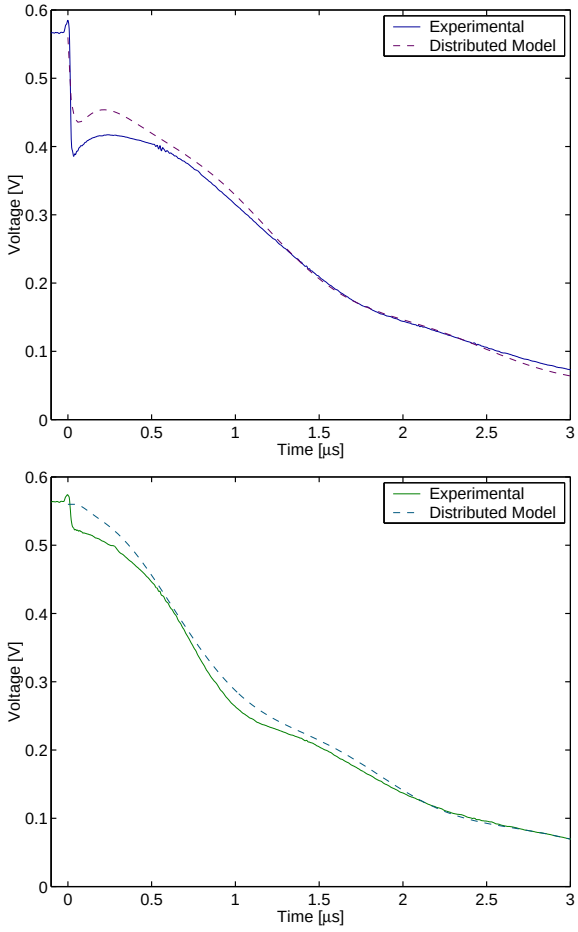

Fig. 4. Comparison of measured 100 μF MLC capacitor voltage to simulations using the improved lossy transmission line model. The left plot shows the voltage at the bottom where the capacitor is soldered to board; the right plot shows the voltage at the top, 3 mm above the board. The simulation uses the model of Fig. 1d with parameter values: $L' = 0.77$ nH/mm, $C' = 39.3$ μF/mm, $R'_D = 8.4$ mΩ·mm, $L'_D = 0.65$ nH·mm, and $R'_S = 231$ $\mu\Omega$/mm.

the first few plates, giving a high resistive drop that then decreases as the current spreads through the capacitor and more of the dielectric resistance is in parallel. The effect is similar with both the model in Fig. 1c and the model in Fig. 1d; the latter is preferred because it makes it possible to simultaneously match different parts of the measured response, each of which require different resistor values in the model of Fig. 1c, and so cannot be simultaneously matched with the simpler model.

The main discrepancies in Fig. 4 are at the very beginning. The top measurement shows a step at that point, which we have not yet been able to explain or model. It may be a measurement artifact, but it was repeatable and stable in our measurements. The high-speed pulse propagation could be due to a drop at high frequencies in either capacitance or inductance. A drop in capacitance could be explained a drop in dielectric constant at high frequencies, but the measurements discussed in Section V

TABLE I

TESTED CAPACITORS

Capacitor	ℓ	w	h	C	C_v	Z_0 (2)	T (calc.)	f_0 (exp.)	ESL (from f_0)
MLC	6 mm	5.3 mm	2.7 mm	100 μF	1160 F/m^3	6.2 mΩ	1240 ns	400 kHz	1.68 nH
Film	27.4 mm	23.5 mm	13 mm	10 μF	1.2 F/m^3				

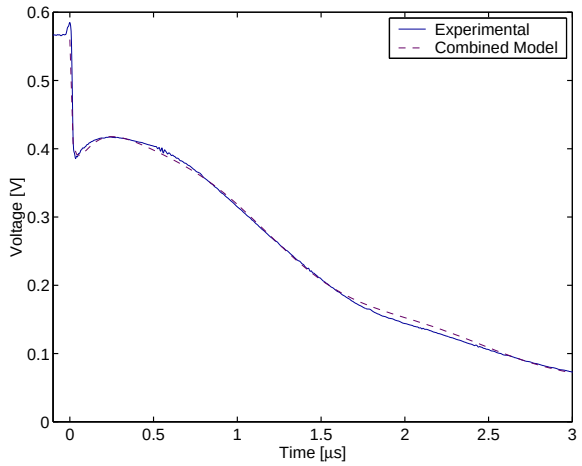

Fig. 5. Combined model for 100 μF MLC capacitor with step-like current waveform compared to experimental results. The simulation uses the model of Fig. 1d with the parameter values in each of 416 sections $L' = 0.77$ nH/mm, $C' = 39.3$ μF/mm, $R'_D = 7.1$ mΩ·mm, $L'_D = 0.65$ nH·mm, $R'_S = 0$ Ω/mm, plus a single lumped external series inductance of 0.3 nH.

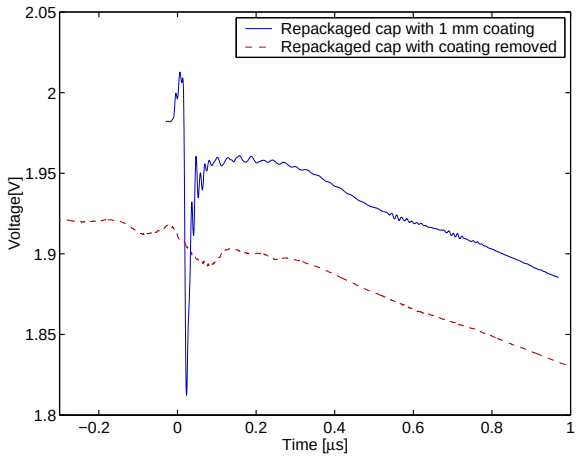

Fig. 6. Measured waveforms on film capacitor.

do not indicate any such drop. A drop in inductance could be the results of magnetically-induced eddy currents within the capacitor plates; this seems to be a more likely explanation.

The discrepancy in the measurement at the bottom terminals of the capacitor is more important, and is, fortunately, easier to explain. The sharpness of the initial spike suggests some ESL, though smaller than the ESL used in the lumped model. Experimentation with different model parameters led to the result shown in Fig. 5 with the improved transmission line model plus an ESL of 0.3 nH. The match to experimental results is excellent with this combined model.

To determine the possible origin of this series inductance, we disassembled a capacitor and found that it has a 0.25 mm thick dielectric coating over the actual capacitor element. According to (1), this introduces 0.36 nH of extra series inductance for the extra path up to the capacitor. Thus, the deviation from the transmission line model is easily explained by the extra lead inductance introduced by the actual physical construction of the capacitor. The transient response could theoretically be improved by reducing the thickness of the coating on the underside of the capacitor.

B. Film Capacitor

Similar behavior can be measured in wound film capacitors. Typical capacitor packages have significant lead inductance, but the capacitor element itself exhibits distributed behavior. In [3], experiments showed that measured inductive spikes are seen with current steps, but the magnitude is much smaller than it would be with the ESL of the whole capacitor. The spike magnitude instead matched that predicted based on the distributed model plus an inductor sized to model only the lead inductance.

Thus, it should be possible to reduce the inductive spike by reducing package inductance; or to nearly eliminate it with very good packaging. To test this, we replaced the leads on a 10 μF polyester film capacitor with wide copper straps and obtained the first voltage waveform shown in Fig. 6 when the capacitor was driven with a current step. However, this still has a small inductive spike. We attributed the spike to the inductance effected by the spacing of the capacitor above the board, due to the 1 mm epoxy coating on it. To test this hypothesis, we removed the coating and repeated the test. As shown in the second waveform in Fig. 6, the spike was almost entirely eliminated. This shows that there are opportunities to make substantial improvements in capacitor performance through improved packaging, based on an understanding of the inductive effects involved.

V. Frequency-Domain Measurements

In principle, frequency-domain and time-domain measurements give equivalent information about the behavior of any linear system. Thus, for our linear models, either approach can be applied. The time domain approach was taken initially, because of the importance of time-domain behavior for power applications. However frequency-domain measurements offer some advantages, including the convenience of using commercially available instruments.

Instruments for frequency-domain impedance measurements fall into two broad categories–impedance analyzers and network analyzers. Network analyzers cover a wide frequency range, but since measurements are referred to a 50 Ω characteristic impedance, they have limited accuracy for the very low impedances we are typically interested in achieving in capacitors for power applications, particularly in microprocessor power delivery applications. Impedance analyzers have a more limited frequency range, but are accurate over a wide range of impedance magnitudes, and so are more suitable for our purposes.

Just as careful circuit layout is critical for doing time-domain measurements, careful test fixture design and calibration is essential for frequency-domain measurements. Standard test fixtures for impedance measurement of surface-mount components have stray inductance of about 100 nH. Although calibration with a short circuit measurement can subtract this fixture inductance, good results cannot be expected when the quantity being subtracted is two orders of magnitude larger than the circa 1 nH inductance of the capacitors we are measuring. High-performance test-fixture design for measuring capacitors with network analyzers are addressed in [7], [8], [9], but these are subject to the limited accuracy at low impedance inherent in the network analyzer approach. To make accurate measurements in a lower impedance range, we used a high performance impedance analyzer (Agilent 4294A) with a new test fixture we developed that has stray inductance on the order of 100 pH, as described in detail in [10].

To construct a model for the 100 μF MLC capacitor systematically using frequency-domain measurements, we wished to first characterize the X5R dielectric material. We did this by measuring a smaller capacitor in which inductive effects were negligible over the frequency range we measured–from 100 kHz to 110 MHz. We used a 4700 pF nominal 0.6 mm × 0.3 mm (EIA 0201) X5R capacitor. This test showed that the dielectric characteristics are in fact much simpler than the shunt portion of the model in Fig. 1.d. The impedance matched that of a constant capacitance with a frequency dependent ESR, and we found that it could be modelled accurately with just a three-element lumped model: a capacitor with series and parallel resistors as shown in Fig. 7. A distributed model is not needed for this capacitor in this frequency range.

We now have sufficient information to derive many of the components of a distributed model for the 100 μF MLC capacitor. We calculate inductance per unit length according to (1). We use the model in Fig. 7, scaled by capacitance, for the shunt path. And we calculate an external inductance also using (1), based on the thickness of the insulating coating on the outside of the capacitor.

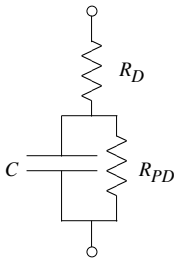

Fig. 7. Model for a small MLC capacitor below resonance. The simple nature of this model indicates that the more complicated model for the shunt path in Fig. 1.d. does not accurately represent dielectric behavior, and that the observed characteristics of larger capacitors must arise as a result of other effects.

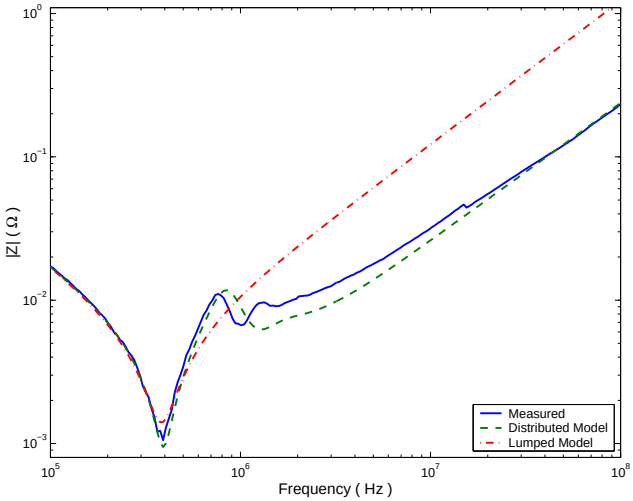

Fig. 8. Measured impedance of a 100 μF MLC capacitor compared to distributed and lumped models. The distributed model is as in Fig. 9; the lumped model is using the datasheet values of ESL = 1.95 nH and ESR = 1.4 mΩ.

However, the model with only the known components as described above exhibits much too little damping to match the measured results shown in Fig. 8. The resistance of the plates is an additional series resistance, that may be directly added to the value of R_D in Fig. 7. Adjusting this value allows matching the measured depth of the first resonance. However, the remaining higher frequency resonances are still much more heavily damped in the measured data than in the model so far. What is needed is additional frequency-dependent damping.

Although it would be possible to add in additional frequency-dependent damping with no physical motivation in order to make the model fit the data, it is preferable to understand the

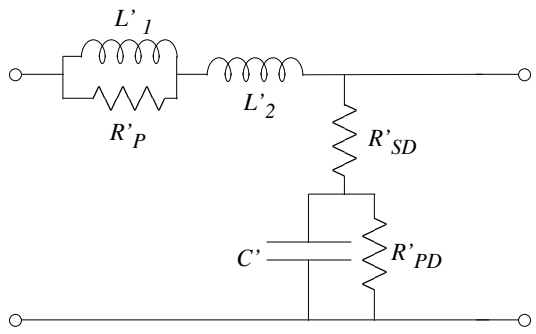

Fig. 9. Distributed model for a 100 μF MLC capacitor developed from frequency-domain data. The values used are $L'_1 = 0.85$ nH/mm, $L'_2 = 0.57$ nH/mm, $C' = 32.6$ μF/mm, $R'_P = 12$ mΩ/mm, $R'_{SD} = 1.2$ mΩ·mm, and $R'_{PD} = 20$ Ω·mm.

physical origin of this effect and add the damping appropriately.

Another source of loss, and thus of damping, is eddy-currents in the plates induced by changing magnetic fields. This is similar to "proximity-effect" in high-frequency magnetic components [11], [12], where it is well-known that a large number of layers–as we have in MLC capacitors—can give rise to substantial proximity effect losses, even when the layers are significantly thinner than a skin depth. In addition, field components perpendicular to planar conductors can induce even greater losses.

A crude model of eddy-current losses in the plates can be obtained by putting a resistor in parallel with the distributed inductance. This results in a loss term that depends upon the square of the voltage across the inductance, which is this also proportional to the square of the derivative of the flux in the inductor, as is appropriate for eddy-current loss. Because only the portion of the flux that goes through the plates, rather than the dielectric, induces losses, the distributed inductance L' is broken into two pieces, L_1 and L_2, and the eddy-current loss resistor R'_E is placed in parallel with only one of them.

With this eddy current loss model, the final distributed model based on frequency-domain measurements is shown in Fig. 9. In this model, C' is based on the measured capacitance, although rated capacitance could also be used. The parallel dielectric loss resistance, R'_{PD}, is based on the measurements of a small capacitor, scaled according to capacitance. It is insignificant except for its effect on ESR below the first resonance, and may be omitted from the model for many purposes, or placed external to the distributed portion of the model. R'_{SD} is much larger than it would need to be to model dielectric loss resistance; it is primarily plate resistance, found based on matching experimental impedance measurements. The total of L'_1 and L'_2 is chosen according to (1). The allocation of total inductance is between L'_1 and L'_2 is not critical, but for a given allocation, the value of R'_P is chosen to approximate the experimentally measured damping of secondary resonances. Not shown in Fig. 9 is the external 0.36 nH inductance, calculated from (1), based on the thickness of the insulating coating on the capacitor.

The resulting model is compared to experimental data and to a simple lumped model in Fig. 8. The distributed model is superior to the lumped model both in capturing more of the qualitative features and in being quantitatively closer to the measured data. The measurement exhibits an impedance a factor five lower than the lumped model predicts over a wide range of high frequencies, whereas the largest error in the distributed model is ten times smaller, and occurs in a much smaller range of frequencies.

Despite the great improvement, the distributed model still differs significantly from the measured data. A more detailed model of the eddy-current losses could probably improve the fit by tailoring the damping as a function of frequency to more accurately match the actual behavior. An interesting characteristic of the measured data is that the resonant frequencies become slightly more closely spaced at higher frequencies, whereas the model's resonances become slightly more widely spaced. This results in a peak in measured impedance matching up with a dip in modelled impedance at 1.3 MHz, giving rise to the largest discrepancy between the two. The measured data could be explained if distributed capacitance or inductance increased with frequency; however, our tests on the small capacitor indicated that the dielectric does not change permittivity in this frequency range, and eddy-current effects would make inductance decrease with frequency rather than increase. More study is needed to determine the physical origin of this effect and to develop a model that takes it into account. It is likely that our one-dimensional model misses some two- and three-dimensional aspects of the real behavior that are responsible for this effect. For example, the accuracy of (1) is reduced when h is not much smaller then w, and the inductance and eddy-current loss become a function of vertical position. We have also assumed that current flows in simple patterns, with equal displacement current density throughout each layer of dielectric, but this may not be the case.

For power applications, loss can be more important than the magnitude of impedance. Thus, we compare the real component of impedance (ESR) of the 100 μF MLC capacitor to that of the distributed and lumped models in Fig. 10. Again, the distributed model is vastly superior both in qualitatively matching characteristics of the measured data and in quantitatively predicting the values. The accuracy of the model degrades at high frequency, indicating that our simple model has not accurately capture the frequency dependence of eddy current losses. However, it provides less than one fifth the error of the simple lumped model.

VI. Application

Although our models do not perfectly match the measured behavior, they match much better than the models presently in use. In particular, ESL can overestimate high-frequency

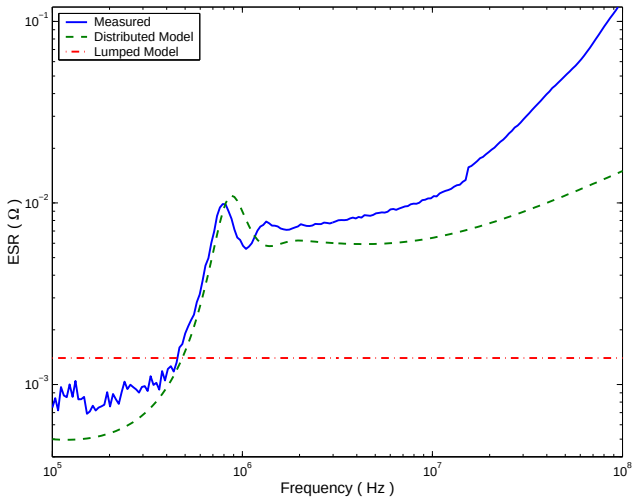

Fig. 10. Measured ESR (real component of impedance) of a 100 μF MLC capacitor compared to distributed and lumped models. The distributed model is as in Fig. 9; the ESR of the lumped model is determined solely by the datasheet value of ESR = 1.4 mΩ.

impedance by a factor of five. Thus, designers faced with designing a system in which capacitor behavior is critical would like to make use of the improved models despite their relatively minor limitations. The model we provide can be used, but it has two limitations for practical use. The first is that is inconvenient to simulate. In our simulations we approximated the distributed model with 416 lumped sections. This was overkill; we now know that a tenth as many sections or less would be an adequate approximation. However, this is still much more complexity than a conventional lumped model and it would make large simulations including many capacitors run slowly. The second disadvantage is that we have developed the model for only one capacitor type. Fortunately, some of the parameters can be calculated from geometry and capacitance. But the distributed eddy-current loss resistance R'_P and the plate resistance R'_{SD} need to be determined by comparing modelled and measured impedance. Capacitor manufacturers could help their customers by to performing the type of modelling we have done here and providing these parameters to their customers, but for now capacitor users are faced with measuring these parameters themselves.

However, even without a complete model, the work reported here facilitates an understanding of the relationship between capacitor construction and the characteristics of the impedance curve in Fig. 8. The curve can be understood as having four regions. In the first region, the behavior is that of an ideal capacitor. Next is the first resonance, for which the lumped model is adequate. Immediately following that resonance, the impedance shows oscillatory behavior, centered around the characteristic impedance. Finally, the curve rises as the external series inductance starts to dominate total impedance. The ESR curve can also be understood similarly. It starts at a low value, similar to the manufacturer's rated value, and then rises abruptly to near the characteristic impedance after the first resonance, and continues a more gentle rise at higher frequencies.

As described above, the behavior can be understood from only five parameters, all of which can be obtained from geometry or manufacturer's data: capacitance, low-frequency ESR, first resonant frequency, characteristic impedance, and external series inductance. Capacitance and low-frequency ESR are provided by manufacturers. The first resonant frequency is provided by manufacturers or may be calculated from manufacturer's rated ESL, provided these have been measured in an appropriate test fixture with low stray inductance and a ground-plane in close proximity to the capacitor. Characteristic impedance can be calculated using (2), and external series inductance is theoretically given by $L_{ext} = \frac{\ell}{w} t_c \mu_0$ where t_c is the thickness of the insulating coating on the capacitor.

We can also consider how these parameters can be improved by selecting or designing a better capacitor geometry. As is already widely understood, increases in capacitor width decrease inductive effects. As we show, this both increases the first resonant frequency, extending capacitive behavior to higher-frequencies, and decreases the characteristic impedance that establishes the impedance magnitude and ESR for frequencies immediately above resonance. We are further show is that increased height and length are roughly equivalent, with either having little effect on characteristic impedance, and either increasing round-trip time.

At high frequencies, the external series inductance or packaging inductance dominates. Based on the theoretical expression $L_{ext} = \frac{\ell}{w} t_c \mu_0$, we see that again, increasing width helps, but overall capacitor height no longer matters. Length and coating thickness are now the two dimensions that can be reduced to improve performance. In particular, reducing coating thickness is attractive, since it does not entail any sacrifice in the volume available to meet the capacitance requirement. Our tests of reducing this coating thickness in film capacitors showed promising results, but initial tests of reducing coating thickness in MLC capacitors has resulted in smaller improvements than expected. Further work is needed to verify and understand these results, and the verify the measured improvement in the film capacitor.

VII. Conclusion

RLC models for capacitors in packaging with low lead inductance give misleading predictions. The actual high-frequency inductance, determined primarily by lead or packaging inductance, is much smaller than the ESL determined from the first resonant frequency. In the 100 μF capacitor we measured, the high-frequency inductance is smaller by about a factor of five. This means that the actual high-frequency impedance is much lower than is predicted by the lumped model, and that the inductive spike when a current step is applied is much lower than is predicted by the lumped model. Both of these results have been confirmed by direct measure-

ments.

A simple lossless transmission line model can help in understanding capacitor behavior, but real capacitors typically have substantial damping and are not accurately modelled by the lossless line. Proper placement of damping in the transmission line model is important in order to get good time-domain or frequency-domain results. Placing distributed resistance in series with the distributed capacitance results in a more accurate model than a standard lossy transmission line with resistance in parallel with the capacitance. Additional damping at higher frequencies can be modelled either in the shunt path or the series path. Measurements of a small capacitor show that the additional damping does not arise in the X5R dielectric, leading to the hypothesis that is due to eddy current losses. A simple model for these losses is a distributed resistance in parallel with the distributed inductance.

Although the models we have presented fit measured data much better than the alternatives, refinements are still needed to fully capture the measured behavior. In particular, a method is needed to explain and model the decreasing spacing of resonant peaks as frequency increases, and a model is needed to capture the increasing loss at high frequencies. Investigations of eddy current losses and two- and three-dimensional effects are likely to yield models that explain both of these phenomena.

The models presented here provides a much better match to measured data than do standard models. Both the detailed models, and the understanding they provide, can be helpful to engineers designing circuits or designing capacitors for high performance with high frequencies or fast current steps.

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